



# LCP1511D

Application Specific Discretes  
A.S.D.<sup>TM</sup>

## PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

### FEATURES

- DUAL PROGRAMMABLE TRANSIENT SUPPRESSOR.
- WIDE NEGATIVE FIRING VOLTAGE RANGE :  
 $V_{MGL} = -80V$  max.
- LOW DYNAMIC SWITCHING VOLTAGES :  
 $V_{FP}$  and  $V_{DGL}$ .
- LOW GATE TRIGGERING CURRENT :  
 $I_{GT} = 5mA$  max.
- PEAK PULSE CURRENT :  
 $I_{PP} = 30A$  for 10/100 $\mu s$  surge.
- HOLDING CURRENT :  
 $I_H = 150mA$ .

### DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

Positive overloads are clipped with 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to  $-V_{BAT}$  through the gate.

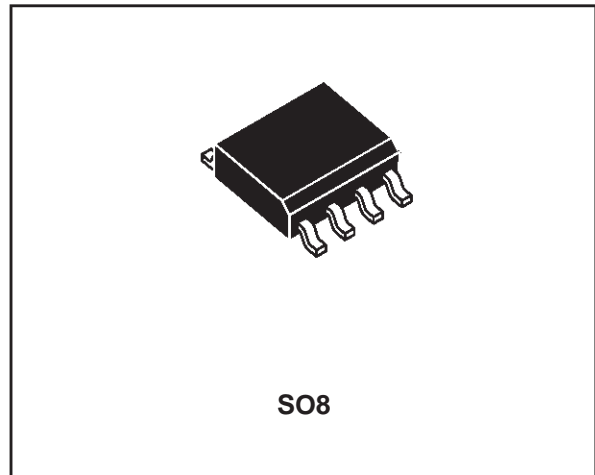
This component presents a very low gate triggering current ( $I_{GT}$ ) in order to reduce the current consumption on printed circuit board during the firing phase.

A particular attention has been given to the internal wire bonding. The "4-point" configuration ensures reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring ( $Ldi/dt$ ), especially for very fast transients.

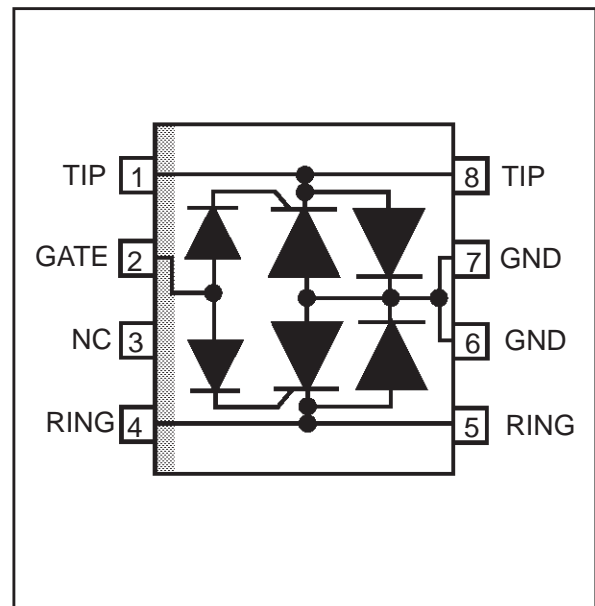
### COMPLIES WITH THE FOLLOWING STANDARDS :

<b>CCITT K20 :</b>	10/700 $\mu s$	1kV
	5/310 $\mu s$	25A
<b>VDE 0433 :</b>	10/700 $\mu s$	2kV
	5/310 $\mu s$	38A (*)
<b>VDE 0878 :</b>	1.2/50 $\mu s$	1.5kV
	1/20 $\mu s$	40A
<b>I3124 :</b>	0.5/700 $\mu s$	1kV
	0.2/310 $\mu s$	25A
<b>FCC part 68 :</b>	2/10 $\mu s$	2.5kV
	2/10 $\mu s$	170A (*)
<b>BELLCORE</b>		
<b>TR-NWT-001089 :</b>	2/10 $\mu s$	2.5kV
	2/10 $\mu s$	170A (*)

(\*) with series resistors or PTC.



### SCHEMATIC DIAGRAM



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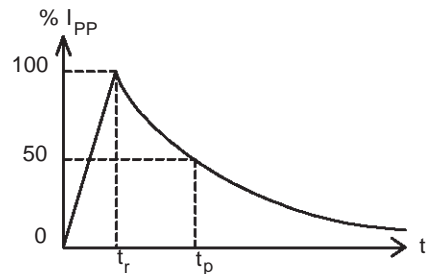
# LCP1511D

## ABSOLUTE MAXIMUM RATINGS (T<sub>amb</sub> = 25 °C)

Symbol	Parameter	Value	Unit	
I <sub>PP</sub>	Peak pulse current (see note 1)	10/1000µs 5/310µs 2/10µs	30 38 170	A
I <sub>TSM</sub>	Non repetitive surge peak on-state current (F = 50Hz)	t <sub>p</sub> = 10ms t = 1s	8 3.5	A
I <sub>GSM</sub>	Maximum gate current (half sine wave t <sub>p</sub> = 10ms)		2	A
V <sub>MLG</sub> V <sub>MGL</sub>	Maximum voltage LINE / GROUND Maximum voltage GATE / LINE		-100 -80	V
T <sub>stg</sub> T <sub>j</sub>	Storage temperature range Maximum junction temperature		- 55 to + 150 150	°C
T <sub>L</sub>	Maximum lead temperature for soldering during 10s		260	°C

Note 1 : Pulse waveform :

10/1000µs	t <sub>r</sub> =10µs	t <sub>p</sub> =1000µs
5/310µs	t <sub>r</sub> =5µs	t <sub>p</sub> =310µs
2/10µs	t <sub>r</sub> =2µs	t <sub>p</sub> =10µs

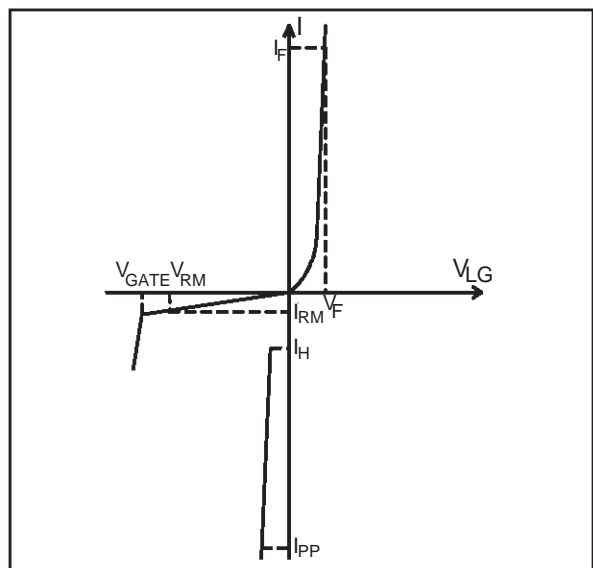


## THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
R <sub>th(j-a)</sub>	Junction to ambient	170	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>amb</sub> = 25 °C)

Symbol	Parameter
I <sub>GT</sub>	Gate triggering current
I <sub>H</sub>	Holding current
I <sub>RM</sub>	Reverse leakage current LINE/GND
I <sub>RG</sub>	Reverse leakage current GATE/LINE
V <sub>RM</sub>	Reverse voltage LINE/GND
V <sub>F</sub>	Forward drop voltage LINE/GND
V <sub>GT</sub>	Gate triggering voltage
V <sub>FP</sub>	Peak forward voltage LINE/GND
V <sub>DGL</sub>	Dynamic switching voltage GATE/LINE
V <sub>GATE</sub>	GATE/GND voltage
V <sub>LG</sub>	LINE/GND voltage
C	Off-state capacitance LINE/GND



**1 - PARAMETERS RELATED TO THE DIODE LINE/GND** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )

Symbol	Test conditions	Maximum	Unit
$V_F$	$I_F=5\text{A}$ $t_p=500\mu\text{s}$	3	V
$V_{FP}$	$10/700\mu\text{s}$ $1.5\text{kV}$ $R_p=10\Omega$ $1.2/50\mu\text{s}$ $1.5\text{kV}$ $R_p=10\Omega$ (see note 1) $2/10\mu\text{s}$ $2.5\text{kV}$ $R_p=62\Omega$	5 7 12	V

**Note 1 :** See test circuit 2 for  $V_{FP}$ ;  $R_p$  is the protection resistor located on the line card.

**2 - PARAMETERS RELATED TO THE PROTECTION THYRISTOR** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )

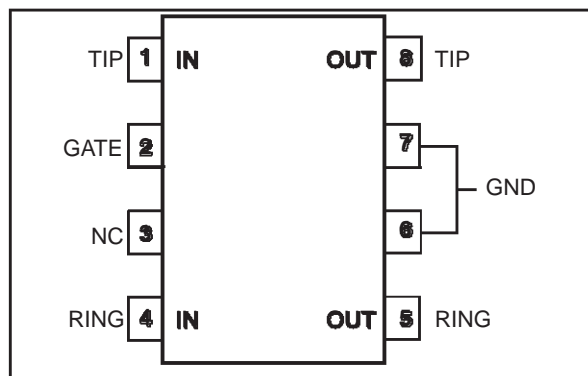
Symbol	Test conditions	Min.	Max.	Unit
$I_{GT}$	$V_{GND/LINE} = -48\text{V}$	0.2	5	mA
$I_H$	$V_{GATE} = -48\text{V}$ (see note 2)	150		mA
$V_{GT}$	at $I_{GT}$		2.5	V
$I_{RG}$	$T_c=25\text{ }^{\circ}\text{C}$ $V_{RG} = -75\text{V}$ $T_c=70\text{ }^{\circ}\text{C}$ $V_{RG} = -75\text{V}$		5 50	$\mu\text{A}$
$V_{DGL}$	$V_{GATE} = -48\text{V}$ (see note 3) $10/700\mu\text{s}$ $1.5\text{kV}$ $R_p=10\Omega$ $I_{PP}=30\text{A}$ $1.2/50\mu\text{s}$ $1.5\text{kV}$ $R_p=10\Omega$ $I_{PP}=30\text{A}$ $2/10\mu\text{s}$ $2.5\text{kV}$ $R_p=62\Omega$ $I_{PP}=38\text{A}$		10 20 25	V

**Note 2 :** See the functional holding current ( $I_H$ ) test circuit 2.

**Note 3 :** See test circuit 1 for  $V_{DGL}$ .  
The oscillations with a time duration lower than 50ns are not taken into account.

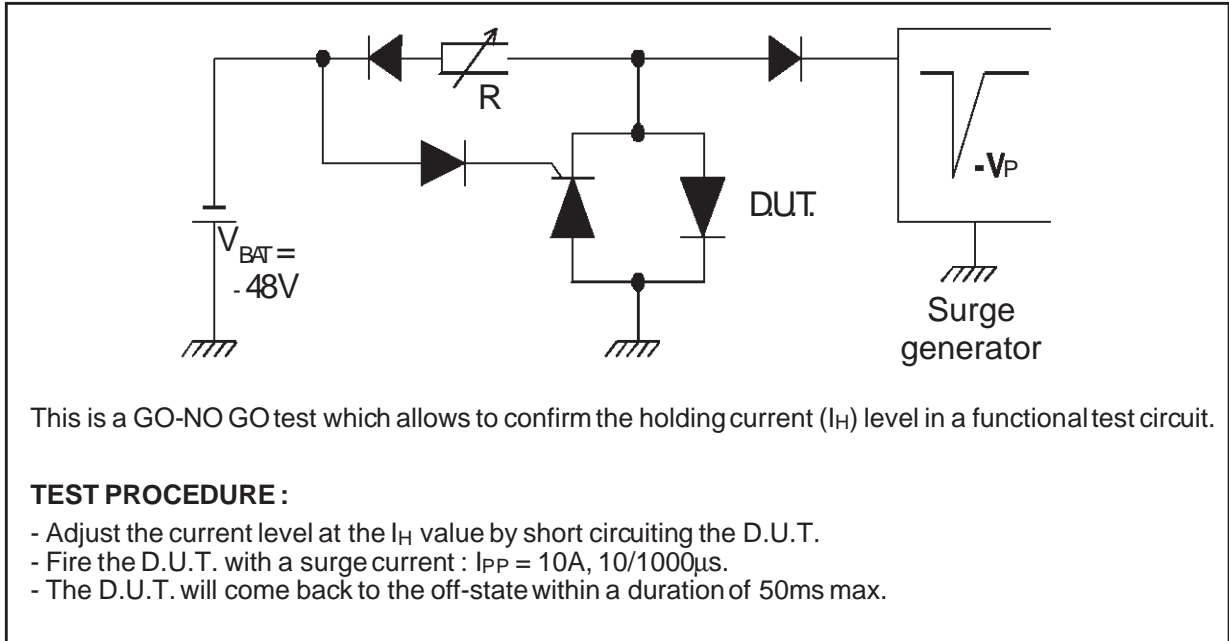
**3 - PARAMETERS RELATED TO DIODE AND PROTECTION THYRISTOR** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )

Symbol	Test conditions	Maximum	Unit
$I_{RM}$	$T_c=25\text{ }^{\circ}\text{C}$ $V_{GATE/LINE} = -1\text{V}$ $V_{RM} = -75\text{V}$ $T_c=70\text{ }^{\circ}\text{C}$ $V_{GATE/LINE} = -1\text{V}$ $V_{RM} = -75\text{V}$	5 50	$\mu\text{A}$
C	$V_R = -3\text{V}$ $F=1\text{MHz}$ $V_R = -48\text{V}$ $F=1\text{MHz}$	100 50	pF

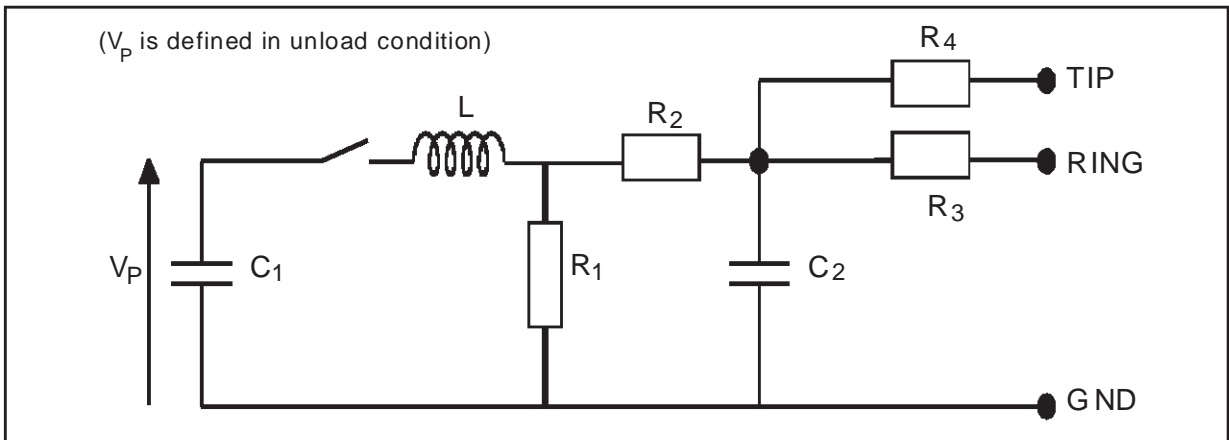
**APPLICATION NOTE**

In order to take advantage of the "4 point" structure of the LCP, the TIP and RING lines go across the device. In such case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring ( $Ldi/dt$ ), especially for very fast transients.

**FUNCTIONAL HOLDING CURRENT ( $I_H$ ) TEST CIRCUIT 1 : GO-NO GO TEST**

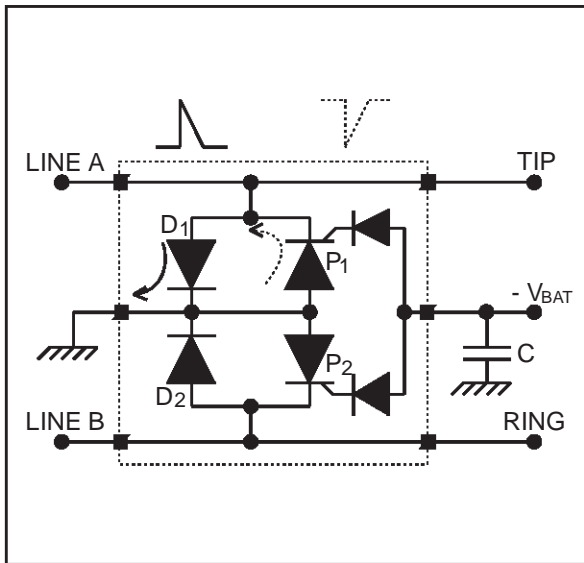


**TEST CIRCUIT 2 FOR  $V_{FP}$  AND  $V_{DGL}$  PARAMETERS**



Pulse ( $\mu s$ )		$V_p$ (V)	$C_1$ ( $\mu F$ )	$C_2$ (nF)	L ( $\mu H$ )	$R_1$ ( $\Omega$ )	$R_2$ ( $\Omega$ )	$R_3$ ( $\Omega$ )	$R_4$ ( $\Omega$ )	$I_{PP}$ (A)	$R_p$ ( $\Omega$ )
$t_r$	$t_p$										
10	700	1500	20	200	0	50	15	25	25	30	10
1.2	50	1500	1	33	0	76	13	25	25	30	10
2	10	2500	10	0	1.1	1.3	0	3	3	38	62

**FUNCTIONAL DESCRIPTION**



**LINE A PROTECTION :**

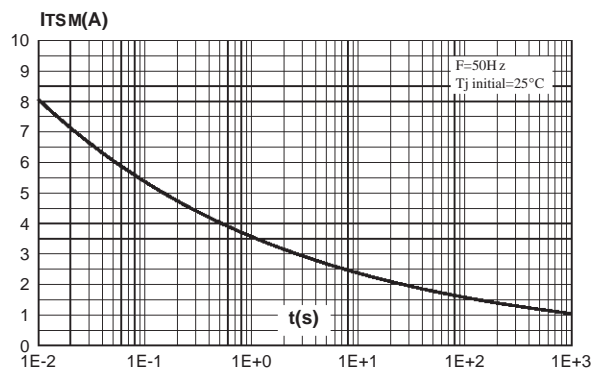
- For positive surges versus GND, the diode D1 will conduct.
- For negative surges versus GND, the protection device P1 will trigger at a voltage fixed by the -V<sub>BAT</sub> reference.

**LINE B PROTECTION :**

- For surges on line B, the operating mode is the same, D2 or P2 is activated.

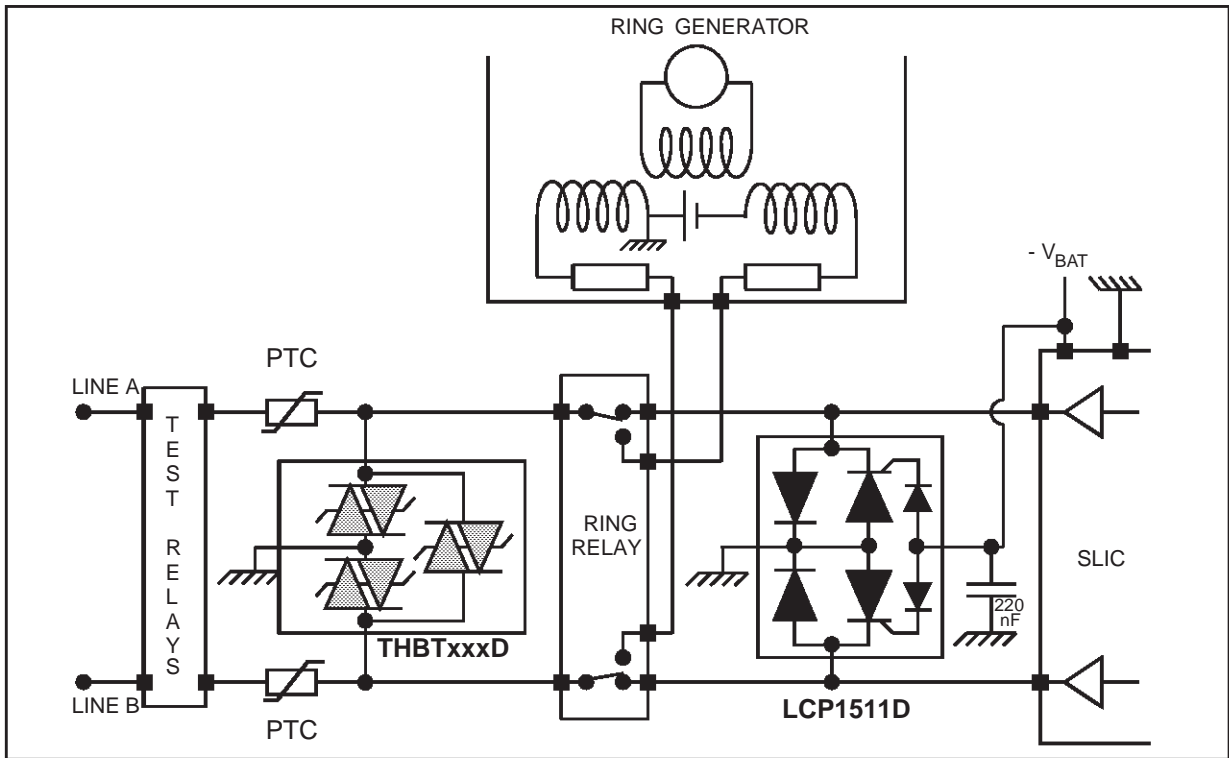
It is recommended to add a capacitor (C=220nF) close to the gate of the LCP, in order to speed up the triggering.

Surge peak current versus overload duration.

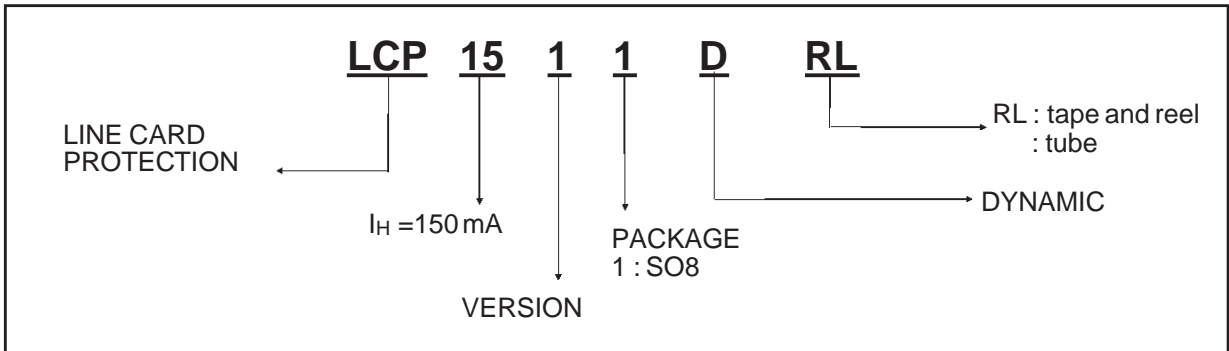


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## APPLICATION CIRCUIT : typical SLIC protection concept



## ORDER CODE

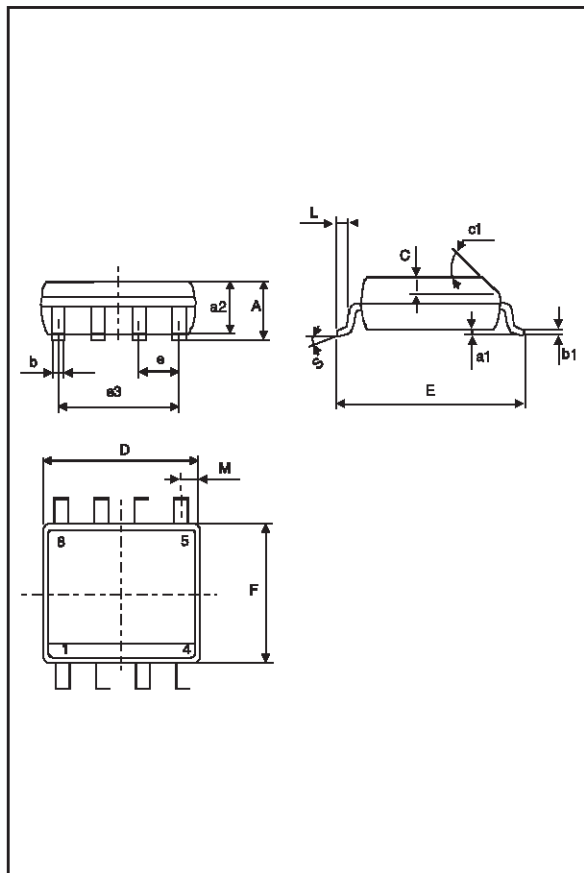


## MARKING

Package	Type	Marking
SO8	LCP1511D	CP151D

**PACKAGE MECHANICAL DATA**

SO8 Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C		0.50			0.020	
c1	45° (typ)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max)					

**Weight** = 0.08 g.**Packaging:** Product supplied in antistatic tubes or tape and reel.

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